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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,414	CARLSON, DAVID W.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7,9,10,13-17,19-25 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9,10,13-17,19-25 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Claims 1, 2, 5-7, 9, 10, 13-17, 19-25 and 27-30 are now pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 19-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 22 recites the limitation "forming a layer of third material on the planarized layer of material, **the third layer of material lowering the resistance of the layer of first material**" in lines 17-18. However there is no support for the limitation "**the third layer of material lowering the resistance of the layer of first material**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 19, 20, 21 and 23 are also rejected as being dependent of the rejected independent base claim.

Applicant's cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 5-7, 10, 13-16, 18-25 and 27-30 rejected under 35 U.S.C. 102(e) as being anticipate by Li et al. (US/6,162,368).

Re claims 1 and 16, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (18) on the top surface of the layer of first material (16), the layer of second material being non-conductive (i.e., an oxide), and having substantially uniform thickness (i.e., the second material layer **18** as shown Figs. 2A and 2B have a uniform thickness); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry to form the planarized

layer of second material (see Figs. 2D-2F); and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of the first material (16) having substantially planar top surface when the layer of second material (18) is substantially all removed (see Fig. 2D) form the layer of first material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 2, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 5, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 6, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the first material as being polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 7, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the second material is being an oxide (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 10 as applied to claim 2 above, Li et al. disclose all the claimed limitations including forming a layer of third material on the planarized layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 13, as applied to claim 12 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 14, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the step of doping the layer of first material prior to forming the layer of second material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 15, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 22, Li et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer (10), the wafer having a top surface (not labeled) , the top surface having a wafer lower level (not labeled) and a wafer upper level (not labeled) that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface (not labeled), the top surface of the layer of first material (16) having a first lower level (not labeled) and a first upper level (not labeled)that lies above the first lower level; forming a layer of second material (18) on the top surface of the layer of first material (16), the layer of second material being non-conductive (i.e., an oxide), and having substantially uniform thickness (i.e., the second material layer **18** as shown Figs. 2A and 2B have a uniform thickness);chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form planarized layer of first material (see Fig. 2D), the

planarized layer of first material (16) covering the wafer upper level (not labeled) of the top surface of the wafer (10), the layer of the first material (16) having substantially planar top surface when the layer of second material (18) is substantially all removed (see Fig. 2D) form the layer of first material; and forming a layer of third material (106 or 114) on the planarized layer of the first material (16) (see Fig. 2D), the third layer of material lowering a resistance of the first layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 19, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 20, as applied to claim 19 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 21, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 23, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 24, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying

above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16), the layer of second material being non-conductive (i.e., an oxide), and having substantially uniform thickness (i.e., the second material layer **18** as shown Figs. 2A and 2B have a uniform thickness); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18) is all removed from the layer of first material (16) to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the layer of the first material (16) having substantially planar top surface when the layer of second material (18) is substantially all removed (see Fig. 2D) form the layer of first material; and forming mask on the planarized layer of material lying over the wafer upper levels and the wafer lower level; selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 25, as applied to claim 24 above, Li et al. disclose all the claimed limitations including forming a layer of third material on the planarized layer of material, the mask being formed on the layer of third material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 27, as applied to claim 24 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material and the layer of second material are etched with a slurry that etches the layer of first material and the layer of second material at approximately a same rate (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 28, as applied to claim 24 above, Lin et al. disclose all the claimed limitations including the limitation wherein all of the layer of second material is removed during the chemically-mechanically polishing step (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 29, Li et al. disclose A method for planarizing a material layer on a processed wafer, the wafer having a top surface, the top surface; having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material on the top surface of the layer of first material, the layer of second material having a substantially uniform thickness (i.e., the second material layer **18** as shown Figs. 2A and 2B have a uniform thickness); and forming a planarized layer of material by chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry, the layer of first material having substantial planar top surface when t the layer of second material is substantially all removed from the layer of first material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of second material having substantially non-planar top surface when polishing begins (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 30, Li et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material on the top surface of the wafer, the layer of first

material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material on the top surface of the layer of first material, the layer of second material bing non-conductive (i.e., an oxide) and having substantially uniform thickness; chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer, the layer of first material having a substantially planar top surface when the layer of second material is substantially removed; and forming a layer of third material on the planarized layer of first material, the third layer of material not contacting the wafer lower level and the wafer upper level see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

6. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Doan et al. (US/6,331,488).

Re claim 17, Doan et al. disclose a method for forming a planarized layer of material on a processed wafer (see Fig. 7), the wafer (20) having a top surface, the top surface having spaced apart wafer (20) upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of forming a layer of first material (24) on the top surface of the wafer (20), the layer of first material (24) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (30) on the top surface of the layer of first material (24), the second layer of material (30) being thicker than the layer of first material (24) and non-conductive (i.e., epoxy material) and having substantially uniform thickness; and chemically-mechanically polishing the layer of

second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of first material (20) having substantially planar top surface (see Fig. 7) when the layer of second material is substantially all removed form the layer of first material (see Figs. 4-7 and related text in Col. 7, line 14 – Col. 10, line 59).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US/6,162,368) in view of Weling et al. (US/5,378,318).

Re claim 9, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (18) on the top surface of the layer of first material (16), the layer of second material being non-conductive (i.e., an oxide), and having a substantially uniform thickness; and chemically-mechanically polishing the layer of

second material (18) and the underlying layer of first material (16) with a slurry to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of first material having a substantially planar top surface when the layer of second material is substantially removed from the layer of first material (see Fig. 2D-2F) (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

However, Li et al. do not specifically disclose the etch selectivity of the first material to the second material being 0.9-1.1:1.

Weling et al. disclose CMP of the first material (21) and second material (23) with a eth selectivity of 1:1, i.e., within the overlap range of the claimed limitation (see Fig. 1, Col. 7, lines 6-11).

Both Li et al. and Weling et al. teachings are directed to CMP process in order to planarize a material for semiconductor device fabrication. Therefore, the teachings Li et al. and Weling et al. are analogous

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Li et al. reference with etch selectivity ratio 1:1 as taught by Weling et al. because in order to polish the first layer and second layer at the same rate and form planar surface for the fabrication of semiconductor device.

Response to Arguments

9. Applicant's arguments filed on January 30, 2004 have been fully considered but they are not persuasive.

With respect to new matter rejection under 35 U.S.C. § 112 first Paragraph, applicant argues that "the specification need not to disclose that which is well-known in the art...Thus, if

the use of material to reduce the resistance of polysilicon is well-known in the art, applicant's specification need not provide examples of those materials..."

In response to applicant's argument, it is respectfully submitted added limitation I claim 22 above has support in the specification as **the specification originally filed**. There is no implicit or explicit reference to third layer, i.e., layer **342** as a material being lowering (reducing) the resistance of the first layer **340** (i.e., the planar polysilicon layer). In addition, if the layer **342** considered to be the material that lower resistance of the polysilicon layer (i.e., for the sake of argument) such claim would have violated the rule that set forth under 35 U.S.C. § 112 first Paragraph for not having enabling disclosure for the material in question because there is no implicit, explicit or exemplary description of the type of the third material that would have ability to reduce the resistance of the polysilicon layer (i.e., the first material). Furthermore, the recited claim is a broad claim and the first and third material layers can be any kind of material. Therefore, it is not known to one having ordinary in the art by placing any type of third material layer over any type of first material layer can reduces or lowers resistance of the first material layer at the time the instant application claimed limitation incorporated into the claim by the way of amendment. Applicant does not provide any evidence to the contrary.

In addition, the case law cited by the applicant is not applicable in this case because the limitation that was rejected under 35 U.S.C. 112 first Paragraph was not introduced in the specification or into the claim at later time via through amendment. It was part of the originally filed disclosure. In this case the limitation introduces into the claim via through amendment, and the claims as being part of the disclosure does not comply with 35 U.S.C. § 132 and also does not comply with 35 U.S.C. § 112 1st Paragraph as containing a new matter which does not enable

to practice the invention at the time the invention made. Therefore, the claims rejection under 35 U.S.C. § 112 first Paragraph is deemed proper.

Applicant further argued that "The CMP shown in Li can not be read to be CMP rqured by the claims. This because the claims required that the layer of first material have a substantial planar top surface when the second layer is substantially removed..."

In response to the applicant's argument, it is respectfully submitted that Li et al. '368 disclose all the claimed limitations the instant application as claimed in claims 1, 22, 24, 29 and 30 and also in claims 19-21, 23, 25 and 27-28 as applied above. For example, as shown in Fig. 2A and presented herein below, the first material layer **16** does not have a planar surface.

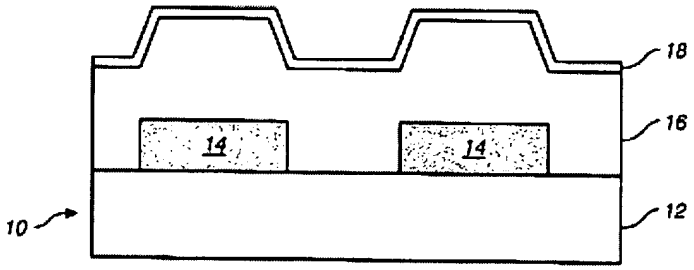

FIG._2A

After the CMP process and removal of the material layer **18**, the first material layer **16** having a substantially planar surface **19** as shown in Fig. 2G herein below.

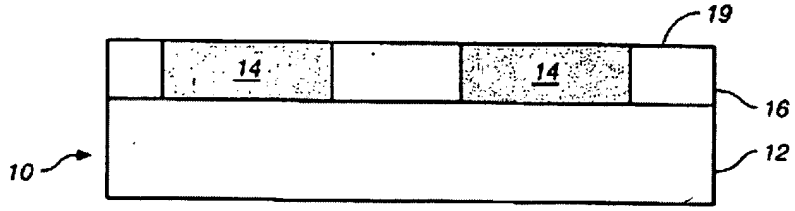

FIG._2G

Therefore, the rejection under 35 U.S.C. §102(e) is deemed proper.

Applicant further argues that "Li fails to teach or suggest formation of third material as claimed in claims 22 and 30..." In repose to applicant's argument, it is respectfully submitted that Li et al. '368 disclose all the claimed limitations of the instant application as claimed in claims 22 and 30 including forming of third material over the planarized second material. For example, Fig. 2I as shown below material layer **114** is meets the claim language third material layer as claimed in claims 22 and 30.

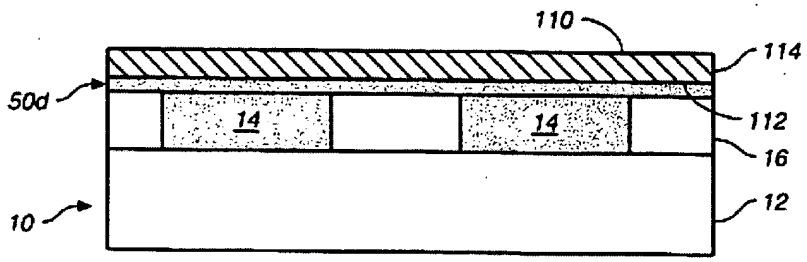

FIG._2I

Furthermore, the rejected claims do not specifically claim the type of material and process step such a way can be distinguishable form Li et al. '368 disclosure. In this regard, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Therefore, the rejection of claims 19-23 under 35 U.S.C. §102(e) is deemed proper.

With respect to claim 24, applicant argues that "Li does not teach forming the masking layer ..."

Prior to responding applicant's contention, the following material facts must be recognized. Formation of the masking layer is added in the claim 24 via through the amendment filed on may 23, 2005 and has no special meaning and considers as third material layer. In order to establish support for this limitation, applicant points out layer **341,** as depicted in Fig. 3C of the instant application, formed over the first material layer **340** is a masking layer. The same layer also claimed as being the third material layer in other claims. However, the claim does not specifically claim the type of material being serve as masking layer as well as how the masking layer is formed. Based on applicants disclosure and broad interpretation of "mask" layer, the determination is made that the the layer 106 or 114 as depicted Figs. 2H and 2I of Li et al. '368 disclosure meet the claim language of claim 24. Therefore, the mask layer nothing more than that of the third layer.

Claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Therefore, the rejection of claim 24 under 35 U.S.C. §102(e) is deemed proper.

With respect to claim 17, applicant argues that "Don reference fails to teach or suggest that deformable material 30 has substantially uniform thickness..."

In response applicant's argument, it is respectfully submitted that Doan et al. '488 disclose all the claimed limitations including the second material layer **30** having substantially uniform thickness as shown in Figs. 5 and 6. The main issue is that claim 17 does not specifically claim the type of material and degree of uniform thickness where and how. Therefore, at any

give location of layer **30** will have uniform thickness. In addition, material layer **30** is a sold resin material layer and applicant's contention that layer **30** is flowing has no merit. One cannot perform a CMP process on liquid material.

Hence, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Therefore, the rejection of claim 24 under 35 U.S.C. §102(e) is deemed proper.

As shown above, the rejection under 35 U.S.C. §102(e) is deemed proper and the rejection of claim 9 under 35 U.S.C. §103(a) also deemed proper and the *prima facie* case of obviousness has been met.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Examiner
Art Unit 2823

BK
August 5, 2005